REMARKS

Claims 3 and 4 are objected to as not showing the claimed step of filtering the nets in the drawings. The examiner is referred to FIG. 6, step 610, which shows the claimed step of filtering the nets.

Claims 1-4, 14-17, and 27 are objected to regarding the terminology ("resistance graph"). Clearly, the terms "resistance" and "graph" are used in the art, and examples of the claimed resistance graph are shown in FIGS. 5A, 5B, and 5C and are described in the specification on page 14, line 5 to page 15, line 4. Further, the rejection under 35 U.S.C. § 102 alleges that the claimed resistance graph is anticipated by the prior art, which may reasonably be construed as an admission that the USPTO considers the claimed resistance graph to be clear and definite.

Claim 27 has been amended to correct the sequence of letters used to reference the steps as suggested by the examiner to satisfy the objection.

Claims 1-27 are pending in the application.

By way of this response, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the examiner telephone Peter Scott at (719)533-7969 so that such issues may be resolved as expeditiously as possible.

Response to the rejection under 35 U.S.C. § 102

Claims 1-27 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by McBride, U.S. Patent No. 6,237,542 (*McBride*). Applicant respectfully traverses the rejection as

follows.

Regarding Claims 1, 14, and 27, the rejection alleges in section 7 that *McBride* teaches parsing the standard parasitic exchange file (20) shown in FIG. 1 and described in column 3, lines 63-67 for finding the resistance of a conductor (702) shown in FIG. 8 and described in column 9, lines 52-56 and column 11, lines 4-7. However, the parasitic file (20) is an input for the static timing analyzer (10) as shown in FIG. 1 and explained by *McBride* in column 3, lines 51-63.

In column 9, lines 52-56, *McBride* describes step (602) of FIG. 7, not step (702) of FIG. 8 as alleged by the rejection. Further, column 11, lines 4-7 cited by the rejection describes step (702) as determining or obtaining a resistance. In column 11, lines 20-22, *McBride* explains that the resistance found in step (702) may be computed separately or from information in a netlist file or other similar software, that is, *McBride* does not teach or suggest that the resistance obtained in step (702) is parsed from the parasitic file (20) in FIG. 1 as alleged by the rejection. Clearly, the rejection errs in alleging a relationship between elements in *McBride* that does not exist. Because *McBride* does not disclose parsing the standard parasitic exchange file to generate a resistance graph as recited in Claims 1, 14, and 27, *McBride* does not anticipate Claims 1-27 under 35 U.S.C. § 102.

The rejection further alleges that *McBride* discloses generating a list of only noise critical nets from the representation of the resistance graph as step (712) in FIG. 8 and in column 1, lines 66-67; column 2, lines 1-17; column 3, lines 26-67; and column 11, lines 35-41. The rejection defines a noise critical net as a net "where the voltage value

exceed[s] a permissible value" to match step (712) in FIG. 8. However, a noise critical net is defined in the specification on page 16, lines 21-25 as follows: "A pin is identified herein to be noise critical if it is a pin of a state cell and if a signal transition on the pin can cause the cell to change state. A net (signal) is identified herein to be noise critical if the net contains a noise critical pin." Clearly the rejection errs in assuming a definition of a noise critical net that is not equivalent to that recited in Claims 1-27. Because the definition of a noise critical net assumed by the rejection is not equivalent to that recited in Claims 1-27, *McBride* does not anticipate Claims 1-27 under 35 U.S.C. § 102.

Further, in column 1, lines 66-67 to column 2, lines 1-17, *McBride* does not mention generating a list of only noise critical nets as alleged by the rejection. In column 3, lines 26-67, *McBride* does not mention generating a list of only noise critical nets as alleged by the rejection. In column 11, lines 35-41, *McBride* does not mention generating a list of only noise critical nets as alleged by the rejection. Because *McBride* does not mention generating a list of only noise critical nets as alleged by the rejection, *McBride* does not anticipate Claims 1-27 under 35 U.S.C. § 102.

The rejection further alleges that *McBride* discloses selecting a victim net from the list of only noise critical nets in column 10, lines 1-9 and column 11, lines 22-27. However, *McBride* does not disclose the claimed list of only noise critical nets as alleged by the rejection. Because *McBride* does not disclose generating a list of only noise critical nets as alleged by the rejection, *McBride* does not anticipate Claims 1-27 under 35 U.S.C. § 102.

Regarding Claims 3 and 16, the rejection alleges in

section 9 that *McBride* discloses filtering the nets in the representation of the resistance graph to exclude nets that are not subject to false switching from crosstalk noise in FIG. 6 and column 8, lines 25-55. However, FIGS. 6A and 6B do not show any filtering to exclude nets that are not subject to false switching from crosstalk noise as alleged by the rejection. Further, column 8, lines 25-55 is directed to computing capacitance and does not disclose filtering nets as alleged by the rejection. As explained in the specification on page 16, line 26 to page 17, line 16, the computation time required for noise analysis may be reduced by filtering out nets that do not require noise analysis. Examples of filters that may be used to filter nets are described on page 17.

Regarding Claims 4 and 17, the rejection alleges in section 10 that *McBride* discloses filtering the nets in the representation of the resistance graph to include nets that drive logical stages that drive noise critical nets in column 13, lines 4-12; FIG. 4 and 5, and column 7, line 63 to column 8, line 24. However, FIGS. 4 and 5 do not show filtering the nets as alleged by the rejection. Further, column 13, lines 4-12 discloses filtering nets to exclude non-problematic nets, not to include nets as recited in Claims 4 and 17. Also, column 7, line 63 to column 8, line 24 is directed to coupling capacitance and resistance circuit models and does not disclose filtering nets as alleged by the rejection. Because *McBride* does not discloses filtering the nets in the representation of the resistance graph to include nets that drive logical stages that drive noise critical nets, *McBride* does not anticipate Claims 1-27 under 35 U.S.C. § 102.

Applicant submits that Claims 1-27 are in condition for allowance and respectfully requests their favorable

examination and reconsideration.

No additional fee is believed due for this amendment.

Respectfully submitted,
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